II. AMENDMENT TO SPECIFICATION

Please amend the specification beginning with the paragraph 0030 on p. 10 as follows:

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Figs. 11-16 illustrate the steps for a forming freestanding semiconductor layer 74 (Fig. 16) on a conventional SOI semiconductor wafer (with base structure 70 and ~~insulator~~ insulating layer 64) shown in cross-section (Figs. 11-15) and plan view (Fig. 16) in accordance with a third embodiment of the present invention. As seen in Fig. 11, the first step 60a is etching aperture 66 through ~~insulator~~ insulating layer 64 to base structure 70. Base structure 70 in this embodiment is an SOI semiconductor wafer that is of a monocrystalline material, such as silicon (Si). Although only one aperture 66 is shown in Fig. 11, the present invention is not limited to such. Other apertures may be formed through ~~insulator~~ insulating layer 64 for multiple contacts of base structure 70 with either mandrel 68 (FIG. 13) or semiconductor layer 72 (FIG. 13).